AMENDMENTS TO THE SPECIFICATION

Please replace Paragraph [0007], which starts with "Please refer to Fig.1…", with the following amended text:

Please refer to Fig. 1. Fig. 1 is a cross-sectional diagram of a prior art typical P-channel flash memory cell 10′ in a programming mode. As shown in Fig. 1, the P-channel flash memory cell 10′ is comprised of an N-type doped substrate 12′, an N-type doped control gate 14′, an N-type doped floating gate 16′, a P^+ source 17′, a P^+ drain 18′, a tunneling oxide layer 21′ located between the floating gate 16′ and the substrate 12′, and an oxide-nitride-oxide (ONO) dielectric layer 22′ located between the control gate 14′ and the floating gate 16′.

Please replace Paragraph [0008], which starts with "In a general band-to-band tunneling (BTBT) programming mode", with the following amended paragraph:

In a general band-to-band tunneling (BTBT) programming mode, a positive high voltage of 10 volts is provided to the control gate 14′, a negative voltage of -6 volts is provided to the drain 18′, the substrate 12′ is grounded, and the source 17′ is in a floating state. In programming mode, electron-hole pairs are generated by band-to-band tunneling in a region where the drain 18′ and the floating gate 16′ overlap. The generated electrons are repelled into the channel region under the floating gate 16′. Some electrons get enough energy to overcome

an energy barrier of the tunneling oxide layer 21' and inject into the floating gat 16'. Please note that programming efficiency and tunneling probability of electrons of the BTBT mechanism are related to an energy gap in the valance band-conduction band (EV-EC) in the region where the drain 18' and the floating gate 16' overlap. The smaller the energy gap is, the greater the band-to-band tunneling probability of electrons will be present.

Please replace Paragraph [0041], which starts with "Please refer to FIG.16…", with the following amended paragraph:

Please refer to FIG.16. FIG.16 illustrates the cross sectional views along lines X_1, X_2, Y_1 and Y_2 of FIG.15, respectively. As shown in FIGS.15 and 16, in X_1 direction, ONO dielectric layer 310 is formed under the word line WL_2, which extends across the active areas 301 and shallow trench isolation (STI) 302. In X_2 direction, it is seen that the source line SL_0 under the STI regions connects the doped source regions 307 of each of the memory cells in one row. An ILD layer is deposited over the substrate. On the top surface of the ILD layer, the bit lines BL_0, BL_1, and BL_2 are formed. As seen in Y_1 direction, the drains 306 of the memory cells in one column are electrically connected to bit line BL_1. The drains 306 are formed in N well 303. As seen in Y_2 direction, the P^+ doping region that connects two neighboring P^+ doped source regions in two adjacent columns is formed after the STI formation. A portion of the STI region between two neighboring P^+ doped source regions, such as S_0 and S_1 as shown in FIG.15, is etched away using a suitable mask. After this, P type dopants are

implanted in the recessed S_0 and S_1 regions, follow d by silicide process, ther by forming the source line SL. The recessed regions are then filled with ILD.

Please replace Paragraph [0043], which starts with "Please refer to FIG.18…", with the following amended paragraph:

Please refer to FIG.18. FIG.18 illustrates the cross sectional views along lines X_1, X_2, Y_1 and Y_2 of FIG.17, respectively. As shown in FIGS.17 and 18, in X_1 direction, ONO dielectric layer 410 is formed under the word line WL_2, which extends across the active areas 401 and shallow trench isolation (STI) 402. In X_2 direction, the local interconnection (LI) source line SL_0 comprising tungsten or metal silicide connects the P^+ doped source regions of the memory cells in the same row. The P^+ doped source regions are formed in N well 403. ILD layers (ILD_1 and ILD_2) are deposited over the substrate. On the top surface of the ILD_2, the bit lines BL_0, BL_1, and BL_2 are formed. As seen in Y_1 direction, the P^+ drains of the memory cells in one column are electrically connected to bit line BL_1 through bit line contacts C_1 and C_2, which are formed in the ILD_1 and ILD_2, respectively. As seen in Y_2 direction, local interconnection source lines SL_0 and SL_1 are formed between WL_0 and WL_1 and between WL_2 and WL_3, respectively.